CHIP-LEVEL OR SYMBOL-LEVEL EQUALIZER STRUCTURE FOR MULTIPLE TRANSMIT AND RECEIVER ANTENNA CONFIGURATIONS

ABSTRACT OF THE DISCLOSURE

Disclosed is a chip-level or a symbol-level equalizer structure for a multiple transmit and receiver antenna architecture system that is suitable for use on the WCDMA downlink. The equalizer structure takes into account the difference in the natures of inter-antenna interference and multiple access interference and suppresses both inter-antenna interference and multiple access interference (MAI). Enhanced receiver performance is achieved with a reasonable implementation complexity. The use of the CDMA receiver architecture, in accordance with this invention, enables the realization of increased data rates for the end user. The CDMA receiver architecture can also be applied in conjunction with space-time transmit diversity (STTD) system architectures.